CLAIMS

What is claimed and desired to be secured by Letters Patent is:

1. A memory device comprising:

a storage element adapted to store data; and

a gated device coupled to said storage element and adapted to set a state of the memory device.

2. The memory device of Claim 1, wherein said gated device comprises at least one gate-ox fuse element.

3. The memory device of Claim 2, wherein said gate-ox fuse element is a thin gate-ox fuse element.

4. The memory device of Claim 3, wherein an oxide of said thin gate-ox fuse element is about 2.5nm thick.

5. The memory device of claim 3, wherein an oxide of said thin gate-ox fuse element is less than about 2.5nm thick.

6. The memory device of Claim 2, wherein said gate-ox fuse element comprises at least two coupled NFet transistors.

7. The memory device of Claim 1, wherein said storage element comprises a 6T storage element.

8. The memory device of Claim 7, wherein said 6T storage element further comprises at two PFet transistors and four NFet transistors.

9. The memory device of Claim 1, including a level shifter adapted to standoff a high voltage required to set said state of the memory device.

10. The memory device of Claim 9, wherein said level shifter includes at least one PFet transistor adapted to standoff said high voltage to at least one other PFet transistor in the memory cell.

11. The memory device of Claim 9, wherein said level shifter includes at least one NFet transistor adapted to standoff said high voltage to at least one other NFet transistor in the memory cell.

12. The memory device of Claim 1, including a programming device adapted to set said state of said memory device.

13. The memory device of Claim 12, wherein said programming device includes at least one switch transistor adapted to select at least one gated device and allow a high voltage to be communicated thereto.

14. The memory device of Claim 12, wherein said programming device includes at least one transistor adapted to keep at least one gated device low when setting said state of the memory device.

15. A one-time programmable memory cell comprising:

a storage element adapted to store data; and

at least one thin gate-ox fuse coupled to said storage element and adapted to set a state of the memory cell.

16. A one-time programmable memory cell comprising:

a storage element adapted to store data;

two gated fuses coupled to said storage element and adapted to set a state of the memory cell;

a level shifter connected to said gated fuses and adapted to stand off a high voltage when setting said state of the memory cell;

at least one switch transistor connected to at least the level shifter and adapted to select at least one of said gated fuses and enable a high voltage to be communicated thereto, setting said state of the memory cell; and

a programming device coupled to said storage element and adapted to keep at least one of the gated fuses low when setting said state of the memory cell.

17. The memory cell of Claim 16, wherein said gated fuses are thin oxide gated fuses.

18. The memory cell of Claim 16, wherein said level shifter includes at least one PFet transistor adapted to standoff said high voltage to at least one other PFet transistor in the memory cell.

19. The memory cell of Claim 16, wherein said level shifter includes at least one NFet transistor adapted to standoff said high voltage to at least one other NFet transistor in the memory cell.

20. A method of setting a state of a memory cell having at least one thin oxide gated fuse comprising rupturing the at least one thin oxide gated fuse.

21. The method of Claim 20, wherein rupturing the thin oxide fuse comprises creating less than about a 6 volt difference across the fuse.

22. The method of Claim 20, wherein rupturing the thin oxide fuse comprises creating about a 5 volt difference across the fuse.